DATA SHEET

TDA8083
Satellite Demodulator and Decoder (SDD3)

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Satellite Demodulator and Decoder (SDD3)

TDA8083

FEATURES

- One chip Digital Video Broadcasting (DVB) (ETS300421) compliant demodulator and concatenated Viterbi and Reed-Solomon decoder with de-interleaver and de-randomizer
- 3.3 V supply voltage
- Relevant outputs are 5 V tolerant to ease interface to 5 V environment
- Few external components for full application
- On-chip crystal oscillator (4 MHz) and Phase-Locked Loop (PLL) for internal clock generation
- Power-on reset module
- QPSK/BPSK demodulator:
  - Different modulation schemes: Quadrature Phase Shift Keying (QPSK) and Binary Phase Shift Keying (BPSK)
  - Interpolator and internal anti-aliasing filter to handle variable symbol rates
  - Tuner Automatic Gain Control (AGC) control
  - Two on-chip matched 7-bit Analog-to-Digital Converters (ADCs)
  - Square-root raised-cosine Nyquist
  - Maximum symbol frequency of 30 Msymbols/s
  - Can be used at low channel Signal-to-Noise Ratio (S/R)
  - Internal full digital carrier recovery, clock recovery and AGC loops with programmable loop filters
  - Two carrier recovery loops enabling optimum phase noise suppression
  - S/R estimation.
- Viterbi decoder:
  - Rate $\frac{1}{2}$ convolutional code based
  - Constraint length K = 7 with $G_1 = 171_{oct}$ and $G_2 = 133_{oct}$
  - Supported puncturing code rates: $\frac{1}{2}$, $\frac{2}{3}$, $\frac{3}{4}$, $\frac{4}{5}$, $\frac{5}{6}$, $\frac{6}{7}$, $\frac{7}{8}$ and $\frac{8}{9}$
  - 4-bit ‘soft decision’ inputs for both I and Q
  - Truncation length of 144
  - Automatic synchronization to detect puncturing rate and spectral inversion
  - Channel Bit Error Rate (BER) estimation from 10^{-2} to 10^{-8}
  - Differential decoding optional.
- Reed-Solomon (RS) decoder:
  - (204, 188, T = 8) Reed-Solomon code
  - Automatic synchronization of bytes, transport packets and frames
  - Internal convolutional de-interleaving (I = 12; using internal memory)
  - De-randomizer based on Pseudo Random Binary Sequence (PRBS)
  - External indication of uncorrectable error (transport error indicator is set)
  - Indication of the number of lost blocks
  - Indication of the number of corrected blocks.
- Interface:
  - I²C-bus interface initializes and monitors the demodulator and Forward Error Correction (FEC) decoder; a default mode is defined
  - 6-bit I/O expander for flexible access to and from the I²C-bus
  - I²C-bus configurable interrupt input
  - Switchable I²C-bus loop-through to suppress I²C-bus crosstalk in the tuner
  - Digital Satellite Equipment Control (DiSEqC) 1.X, tone burst generation and tone mode with a 22 or 44 kHz carrier
  - Parallel or serial output mode for MPEG transport stream (3-state mode also possible)
  - Standby mode for reduced power consumption.
- Package: QFP100
- Boundary scan test.

APPLICATIONS

- Digital satellite TV: demodulation and FEC.

GENERAL DESCRIPTION

This document specifies a DVB compliant demodulator and forward error correction decoder IC for reception of QPSK or BPSK modulated signals for satellite applications. The Satellite Demodulator and Decoder (SSD) can handle variable symbol rates without adapting the analog filters within the tuner. Typical applications for this device are:

- **MCPC (Multi-Channel Per Carrier)**: one QPSK or BPSK modulated signal in a single satellite channel (transponder)
- **Simul-cast**: QPSK or BPSK modulated signal together with a Frequency Modulated (FM) signal in a single satellite channel (transponder).

The TDA8083 can handle variable symbol rates in the range of 12 to 30 Msymbols/s with a minimum number of low cost and non-critical external components.

The TDA8083 has minimal interfaces with the tuner. It only requires the demodulated analog I and Q baseband input signals and provides a tuner AGC control signal. Analog-to-digital conversion is done internally by two matched 7-bit ADCs.

The TDA8083 runs on a low frequency crystal which is upconverted to a clock frequency by means of an internal PLL. Furthermore, the TDA8083 has an internal anti-alias filter, which can cover the range of symbol frequencies without the need to switch external (SAW) filters.

The TDA8083 has a double carrier loop configuration which has excellent capabilities of tracking phase noise. Synchronization of the FEC unit is done completely internally, thereby minimizing I^2C-bus communication. The output of the TDA8083 allows different output modes (parallel or serial) to interface to a demultiplexer, descrambler or MPEG-2 decoder including a 3-state mode. For evaluation of the TDA8083, demodulator and Viterbi decoder outputs can be made available externally.

The SDD can be controlled and monitored by the I^2C-bus. A 5-bit bidirectional I/O expander and an interrupt line are available. By sending an interrupt signal, the SDD can inform the microcontroller of its internal status. Separate resets are available for logic only, logic plus the I^2C-bus and carrier loops. A switchable I^2C-bus loop-through to the tuner is implemented to switch off the I^2C-bus connection to the tuner. This reduces phase noise in the tuner in case of I^2C-bus crosstalk.

Furthermore, for dish control applications hardware supports DiSEqC 1.X and tone burst generation via I^2C-bus control. A 22 or a 44 kHz carrier can be generated (tone mode).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
$I_{DD(tot)}$	total supply current	note 1	–	270	340	mA
$f_{clk(int)}$	internal clock frequency		–	–	64	MHz
r_s	symbol rate		12	–	30	Msymbols/s
α_{ro}	Nyquist roll-off		–	35	–	%
IL	implementation loss	note 2	–	0.3	–	dB
S/R	signal-to-noise ratio	locking the SDD in QPSK mode; note 2	2	–	–	dB
P_{tot}	total power dissipation	T_{amb} = 70 °C; note 1	–	890	1220	mW
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	ambient temperature		0	–	70	°C
T_j	junction temperature	T_{amb} = 70 °C	–	–	125	°C

Notes

1. Typical value is specified for a symbol rate of 27.5 Msymbols/s, a puncture rate of $^3/_4$ and a supply voltage of 3.3 V. Maximum value is specified for a symbol rate of 30 Msymbols/s, a puncture rate of $^7/_8$, a supply voltage of 3.6 V and using a 4 MHz crystal.
2. Implementation loss at the demodulator output and minimum SNR to lock the TDA8083 are measured including tuner in a laboratory environment at a symbol rate of 27.5 MS/s.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8083H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body $14 \times 20 \times 2.8$ mm	SOT317-2

BLOCK DIAGRAM

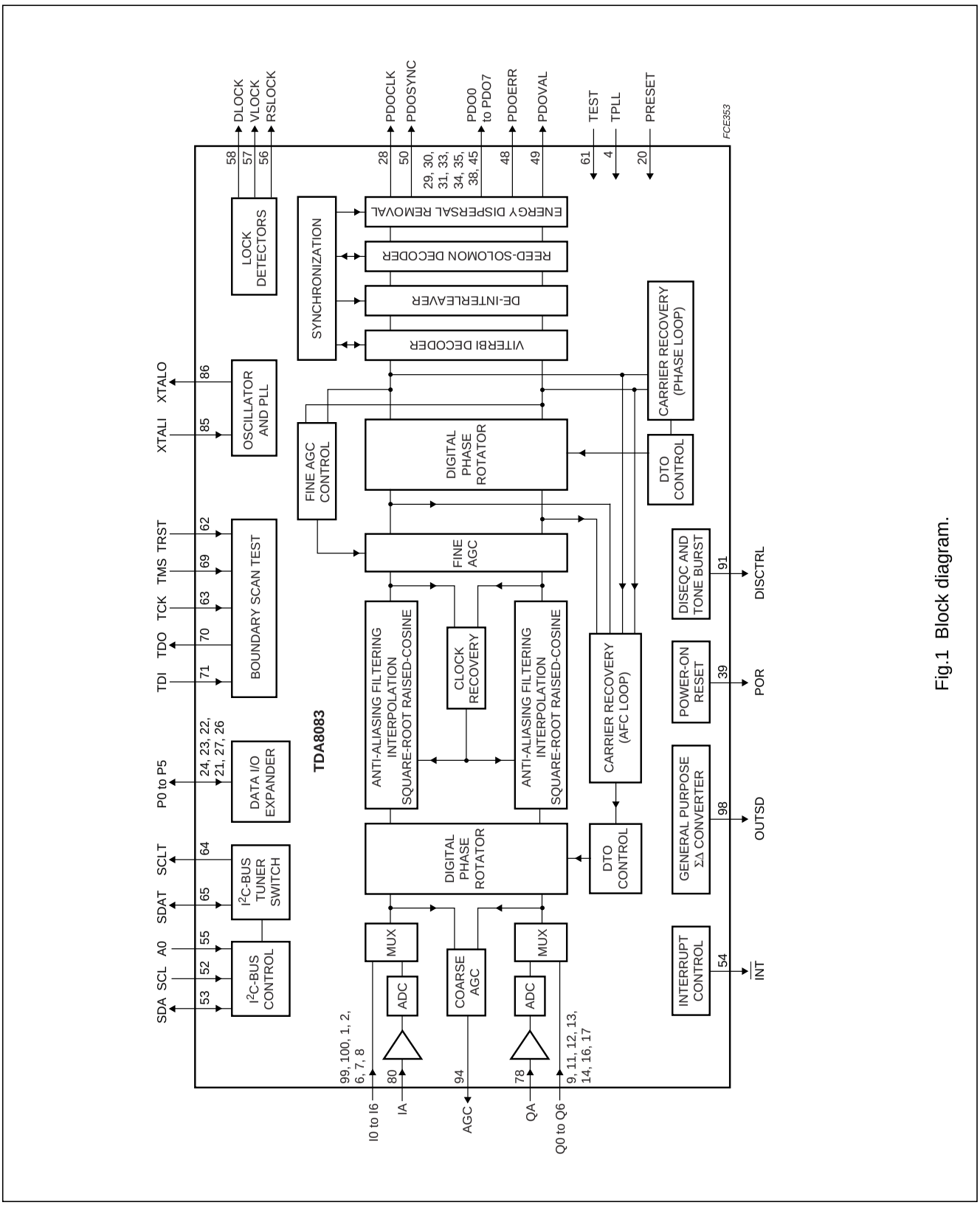


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
I2	1	I	digital I-input bit 2 (ADC bypass); note 1
I3	2	I	digital I-input bit 3 (ADC bypass); note 1
V_{SSD1}	3	–	digital ground 1 (core and input periphery)
TPLL	4	I	test pin (normally connected to ground)
V_{SSD2}	5	–	digital ground 2 (core and input periphery)
I4	6	I	digital I-input bit 4 (ADC bypass); note 1
I5	7	I	digital I-input bit 5 (ADC bypass); note 1
I6	8	I	digital I-input bit 6 (ADC bypass; MSB); note 1
Q0	9	I	digital Q-input bit 0 (ADC bypass; LSB); note 1
V_{DDD1}	10	–	digital supply voltage 1 (core and input periphery)
Q1	11	I	digital Q-input bit 1 (ADC bypass); note 1
Q2	12	I	digital Q-input bit 2 (ADC bypass); note 1
Q3	13	I	digital Q-input bit 3 (ADC bypass); note 1
Q4	14	I	digital Q-input bit 4 (ADC bypass); note 1
V_{SSD3}	15	–	digital ground 3 (core and input periphery)
Q5	16	I	digital Q-input bit 5 (ADC bypass); note 1
Q6	17	I	digital Q-input bit 6 (ADC bypass; MSB); note 1
V_{SSD4}	18	–	digital ground 4 (output periphery)
V_{DDD2}	19	–	digital supply voltage 2 (core and input periphery)
PRESET	20	I	input for default mode setting
P3	21	I/O	quasi-bidirectional I/O port (bit 3)
P2	22	I/O	quasi-bidirectional I/O port (bit 2)
P1	23	I/O	quasi-bidirectional I/O port (bit 1)
P0	24	I/O	quasi-bidirectional I/O port (bit 0)
V_{DDD3}	25	–	digital supply voltage 3 (output periphery)
P5	26	I/O	quasi-bidirectional I/O port (bit 5)
P4	27	I/O	quasi-bidirectional I/O port (bit 4)
PDOCLK	28	O	clock output for transport stream bytes
PDO0	29	O	parallel data output (bit 0) or serial data output
PDO1	30	O	parallel data output (bit 1)
PDO2	31	O	parallel data output (bit 2)
V_{SSD5}	32	–	digital ground 5 (output periphery)
PDO3	33	O	parallel data output (bit 3)
PDO4	34	O	parallel data output (bit 4)
PDO5	35	O	parallel data output (bit 5)
V_{SSD6}	36	–	digital ground 6 (core and input periphery)
V_{SSD7}	37	–	digital ground 7 (core and input periphery)
PDO6	38	O	parallel data output (bit 6)
POR	39	O	Power-on reset output
V_{DDD4}	40	–	digital supply voltage 4 (output periphery)

SYMBOL	PIN	I/O	DESCRIPTION
V_{DDD5}	41	–	digital supply voltage 5 (core and input periphery)
V_{SSD8}	42	–	digital ground 8 (core and input periphery)
V_{DDD6}	43	–	digital supply voltage 6 (core and input periphery)
V_{DDD7}	44	–	digital supply voltage 7 (output periphery)
PDO7	45	O	parallel data output (bit 7)
n.c.	46	–	not connected
V_{SSD9}	47	–	digital ground 9 (core and input periphery)
PDOERR	48	O	transport error indicator output
PDOVAL	49	O	data valid indicator output
PDOSYNC	50	O	transport packet synchronization pulse output
V_{SSD10}	51	–	digital ground 10 (output periphery)
SCL	52	I	serial clock of I^2C-bus input; note 1
SDA	53	I/O	serial data of I^2C-bus input or output; note 1
$\overline{INT}$	54	O	interrupt output (active LOW); note 1
A0	55	I	I^2C-bus hardware address input
RSLOCK	56	O	Reed-Solomon lock indicator output
VLOCK	57	O	Viterbi lock indicator output
DLOCK	58	O	demodulator lock indicator output
V_{DDD8}	59	–	digital supply voltage 8 (core and input periphery)
V_{DDD9}	60	–	digital supply voltage 9 (core and input periphery)
TEST	61	I	test pin (normally connected to ground)
TRST	62	I	BST optional asynchronous reset input (normally connected to ground)
TCK	63	I	BST dedicated test clock input (normally connected to ground)
SCLT	64	O	serial clock of I^2C-bus loop-through output; note 1
SDAT	65	I/O	serial data of I^2C-bus loop-through input or output; note 1
V_{DDD10}	66	–	digital supply voltage 10 (core and input periphery)
V_{SSD11}	67	–	digital ground 11 (output periphery)
V_{SSD12}	68	–	digital ground 12 (core and input periphery)
TMS	69	I	BST control signal input (normally connected to ground)
TDO	70	O	BST serial test data output
TDI	71	I	BST serial test data input (normally connected to ground)
V_{DDD11}	72	–	digital supply voltage 11 (core and input periphery)
V_{SSD13}	73	–	digital ground 13 (core and input periphery)
$V_{SSD(AD)}$	74	–	digital ground ADC
$V_{DDD(AD)}$	75	–	digital supply ADC
$V_{ref(B)}$	76	O	bottom reference voltage output for ADC
V_{SSA1}	77	–	analog ground 1
QA	78	I	analog input Q
$V_{ref(Q)}$	79	O	AGC decoupling output (Q path)
IA	80	I	analog input I
V_{SSA2}	81	–	analog ground 2

SYMBOL	PIN	I/O	DESCRIPTION
$V_{ref(I)}$	82	O	AGC decoupling output (I path)
V_{DDA}	83	–	analog supply voltage
$V_{DD(XTAL)}$	84	–	supply voltage for crystal oscillator
XTALI	85	I	crystal oscillator input
XTALO	86	O	crystal oscillator output
$V_{SS(XTAL)}$	87	–	ground for crystal oscillator
V_{DDD12}	88	–	digital supply voltage 12 (core and input periphery)
V_{DDD13}	89	–	digital supply voltage 13 (core and input periphery)
V_{SSD14}	90	–	digital ground 14 (core and input periphery)
DISCTRL	91	O	22 or 44 kHz output for dish control applications
V_{SSD15}	92	–	digital ground 15 (output periphery)
V_{SSD16}	93	–	digital ground 16 (core and input periphery)
AGC	94	O	tuner AGC output; note 1
n.c.	95	–	not connected
V_{DDD14}	96	–	digital supply voltage 14 (output periphery)
V_{DDD15}	97	–	digital supply voltage 15 (core and input periphery)
OUTSD	98	O	sigma delta output; note 1
I0	99	I	digital I-input bit 0 (ADC bypass; LSB); note 1
I1	100	I	digital I-input bit 1 (ADC bypass); note 1

Note

1. This pin is 5 V tolerant.

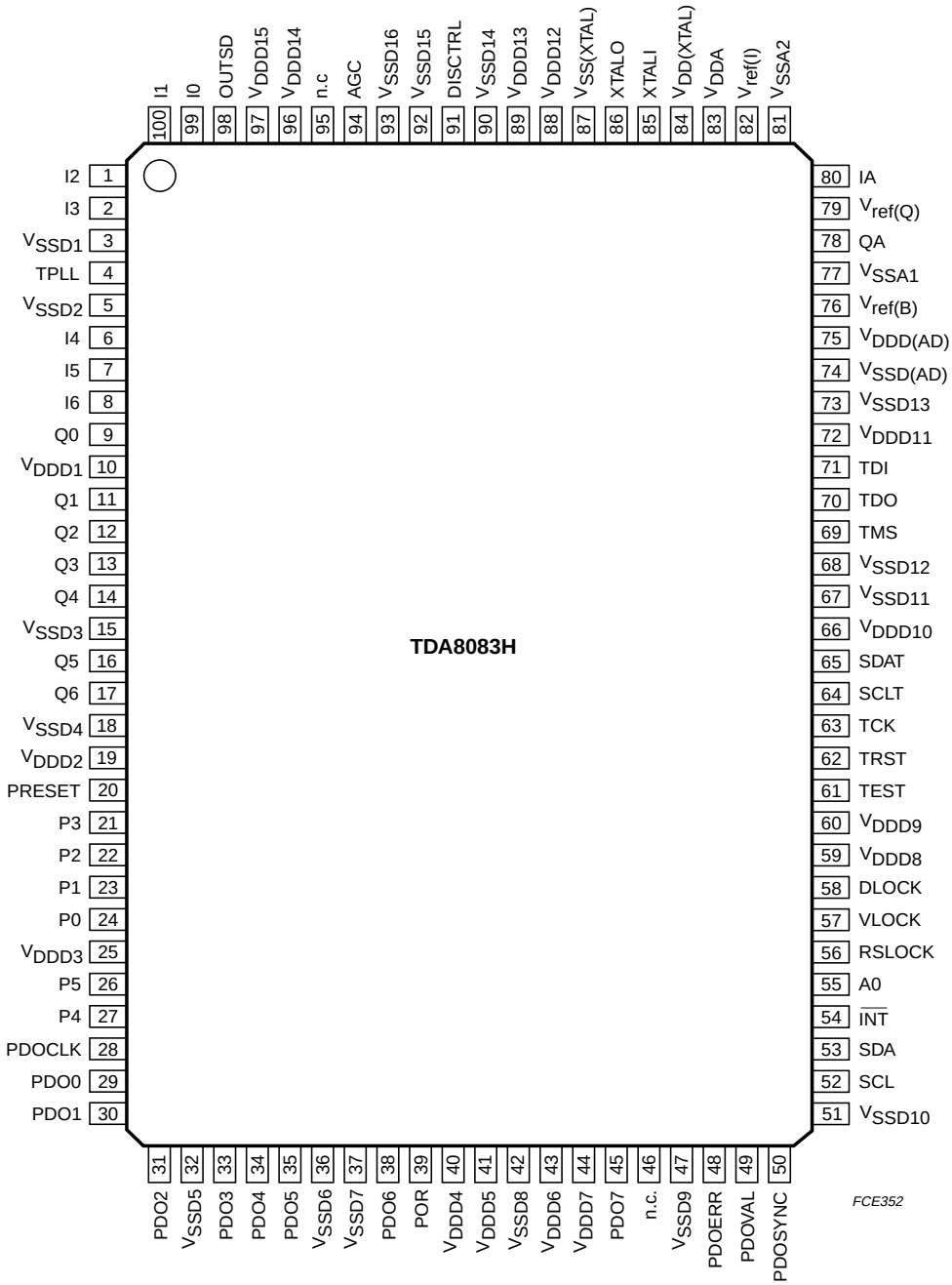


Fig.2 Pin configuration.

APPLICATION INFORMATION

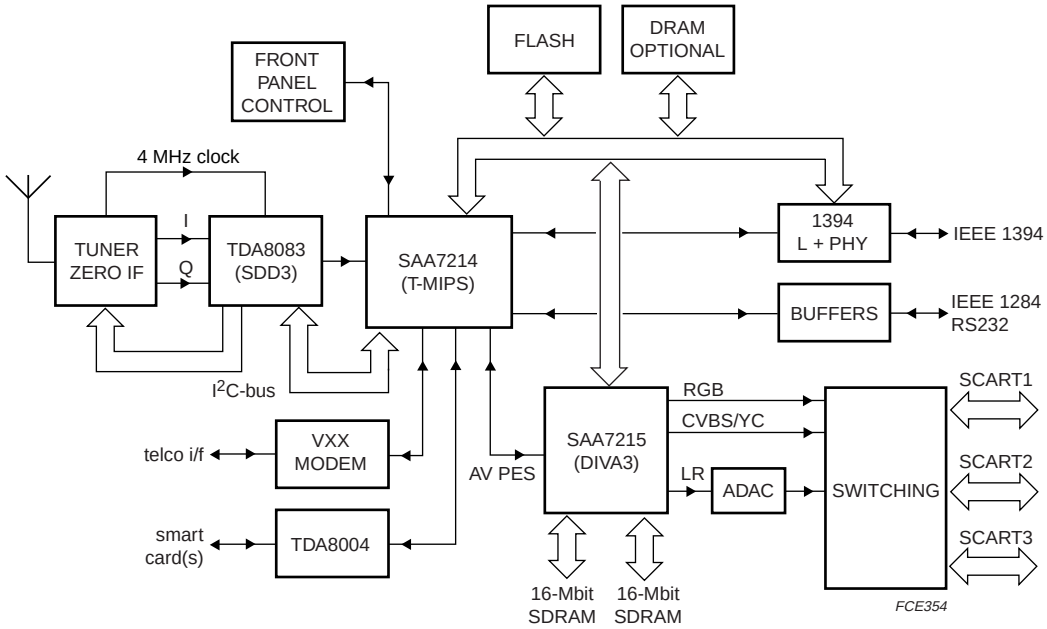
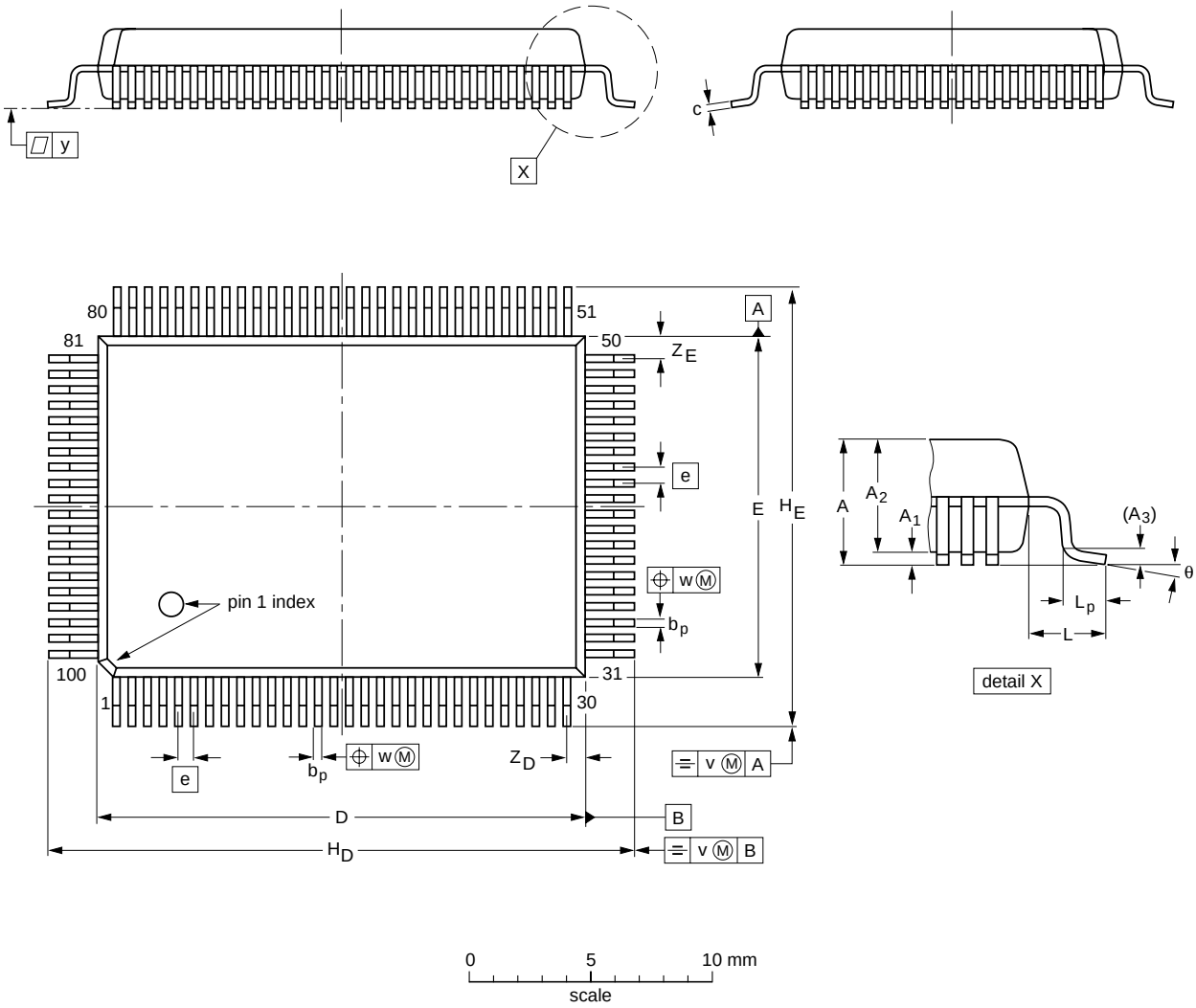


Fig.3 Satellite set-top box concept.

PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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